REMARKS

I. Status Of Claims

Claims 1 and 3-17 are pending in the instant application. Claims 6 and 9 are amended herein. Therefore, upon entry of this Amendment, Claims 1 and 3-17 will be pending. No new matter has been introduced by the present amendment. Reconsideration of the application as amended and based on the arguments set forth hereinbelow is respectfully requested.

II. Claim Objections

The Examiner has objected to Claim 6 because it is contended that the phrase "a negative signal pulse at the output terminal" should be changed to the phrase "a negative signal pulse (logic 0) at the output terminal". Official Action, page 2. Claim 6 has been amended to replace the phrase "a negative signal pulse at the output terminal" with the phrase "the negative signal pulse at the output terminal". In view of the amendment, applicant respectfully submits that the objection to Claim 6 should be withdrawn.

II. Claim Rejections Under 35 U.S.C. §102(b)

Claims 6 and 9 stand rejected by the Examiner under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,111,080 to Mizukami et al. (hereinafter, "Mizukami").

Applicant respectfully traverses the rejection and submits that the claims are allowable over the cited art for the following reasons.

The Examiner contends that Figure 3 of Mizukami teaches all of the features recited in Claims 6 and 9. Official Action, page 3. Upon careful consideration and review of Mizukami, applicant respectfully submits that Mizukami does not disclose each and every feature recited in Claims 6 and 9 and therefore does not anticipate Claims 6 and 9. For example, Claim 6 recites a circuit comprising first and second transistors including first and second control terminals, respectively. In addition, Claim 6 recites that the first and second control terminals are independently controllable. Applicant respectfully submits that Mizukami does not teach a circuit having first and second control terminals that are independently controllable. Referring to Figure 3 of Mizukami, for example, the inputs of transistors **Q1** and **Q2** are coupled to the same input signal **IN**. Therefore, the inputs to transistors **Q1** and **Q2** are not independently controllable because of their connection to a single input signal **IN**. Thus, applicant respectfully submits that Mizukami does not disclose a first and second transistor including control terminals that are independently controllable. Therefore, applicant further urges that Mizukami does not disclose each and every feature recited in Claim 6 and that the rejection of Claim 6 under 35 U.S.C. § 102(b) should be withdrawn.

Similar to Claim 6, Claim 9 recites a circuit comprising first and second transistors including first and second control terminals, respectively. In addition, Claim 9 recites that the first and second control terminals are independently controllable. As noted

above, Mizukami does not teach first and second control terminals that are independently controllable. Therefore, for the reasons similar to those provided for Claim 6, applicant respectfully submits that Mizukami does not disclose each and every feature recited in Claim 9 and that the rejection of Claim 9 under 35 U.S.C. § 102(b) should be withdrawn.

Further, Claim 9 recites a pull-down resistor connected between a second supply potential and the output terminal for generating a positive signal pulse at the output terminal in response to the control terminals receiving the sequence of negative and positive control pulses. Applicant respectfully submits that Mizukami does not disclose a pull-down resistor connected between a second supply potential and the output terminal for generating a positive signal pulse at the output terminal in response to the control terminals receiving the sequence of negative and positive control pulses. Referring to Figure 3 of Mizukami, there is no disclosure of a resistor connected between a second supply potential (i.e., ground) and the output terminal of transistors **Q1** and **Q2**. Therefore, for these additional reasons, applicant further urges that Mizukami does not disclose each and every feature recited in Claim 9 and that the rejection of Claim 9 under 35 U.S.C. § 102(b) should be withdrawn and the claims allowed at this time.

For the reasons provided above, applicant submits that Mizukami does not disclose each and every feature of Claims 6 and 9. Therefore, applicant respectfully submits that the rejection of Claims 6 and 9 under 35 U.S.C. §102(b) should be withdrawn and the claims allowed at this time.

III. Claim Rejections Under 35 U.S.C. §103(a)

The Examiner has rejected Claims 1, 3, 7, 8, 10, and 11 under 35 U.S.C. §103(a) as being unpatentable over Mizukami in view of U.S. Patent No. 5,926,050 to Proebsting (hereinafter, "Proebsting"). Further, the Examiner has rejected Claims 4, 5, and 15-17 under 35 U.S.C. §103(a) as being unpatentable over Mizukami in view of Proebsting and further in view of U.S. Patent No. 6,160,416 to Taguchi (hereinafter, "Taguchi"). These rejections are respectfully traversed.

III.A. The Rejection Under 35 U.S.C. §103(a) Over Mizukami In View of Proebsting

Regarding Claim 1, the Examiner contends that Figure 3 of Mizukami teaches all of the claimed features except for providing a waiting time between the first control pulse and the second control pulse such that the two pulses do not overlap. Official Action, page 4. The Examiner contends that Figures 1 and 2 of Proebsting teaches a waiting time ($\Delta t2 - \Delta t1$) provided between a first control pulse **26'** and a second control pulse **26''** such that the two pulses do not overlap. Official Action, pages 4 and 5. Further, the Examiner contends that it would have been obvious to one of ordinary skill in the art to combine the teachings of Mizukami and Proebsting to arrive at Claim 1. Official Action, page 5.

Claim 3 depends from Claim 1. Claim 1 recites (1) an integrated circuit comprising a push-pull driving circuit having a first and second transistor including control terminals being controllably independent by different control pulses between a first and second supply potential; and (2) a single resistor being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type, wherein the type of the resistor determines, by application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal. Summarily, neither Mizukami nor Proebsting, alone or in combination, discloses (1) an integrated circuit comprising a push-pull driving circuit having a first and second transistor including control terminals being controllably independent by different control pulses between a first and second supply potential; and (2) a single resistor being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type, wherein the type of the resistor determines, by application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal.

As noted above, Claim 1 recites transistors having first and second control terminals that are independently controllable. As stated above, Mizukami does not

disclose transistors having first and second control terminals that are independently controllable. Moreover, Mizukami does not suggest modifying the circuit described therein to achieve a circuit including transistors having first and second control terminals that are independently controllable.

Further, as noted above, Mizukami does not disclose a resistor being of a pull-up or pull-down type that determines, by application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal. The Examiner contends that resistor **R4** of Figure 3 determines, by application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal. Official Action, page 4. Mizukami provides no disclosure or suggestion of resistor **R4** being used as a pull-up resistor for determining, by application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal. In addition, as noted above, resistor **R4** cannot operate as a pull-down because of its connection to supply voltage $\mathbf{V_{DD}}$.

Proebsting fails to overcome the significant shortcomings of Mizukami. For example, Proebsting does not disclose or suggest transistors having first and second control terminals that are independently controllable. Referring to Figure 1 of Proebsting, first and second data paths **20** and **22** having different delay are shown. However, these data paths **20** and **22** are not independently controllable because they are both receive signaling from at a first circuit node **12** from input signal V_i. For these reasons, it is respectfully submitted that the rejection of independent Claim 1 and dependent Claim 3 should now be withdrawn. Additionally, Proebsting offers no suggestion to modify the circuit disclosed therein to arrive at the presently claimed invention and, consequently, the combination proposed by the Examiner does not offer a reasonable chance of success in combining the cited references.

Further, Proebsting does not disclose application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor. Referring to Figure 2 of Proebsting, output signal V_0 and V_0' of first and second data paths **20** and **22** are shown overlapping one another. Therefore, Proebsting does not disclose application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor. For these additional reasons, it is also respectfully submitted that the rejection of independent Claim 1 and dependent Claim 3 should now be withdrawn. Additionally, Proebsting offers no suggestion to modify the circuit disclosed therein to arrive at the presently claimed invention and, consequently, the combination proposed

by the Examiner does not offer a reasonable chance of success in combining the cited references.

As stated above, Claim 3 depends from Claim 1. Therefore, the comments presented above relating to Claim 1 apply equally to Claim 3.

Claims 7 and 8 depend from Claim 6. Claims 10 and 11 depend from Claim 9. Claims 6 and 9 recite a circuit comprising first and second transistors including first and second control terminals, respectively. In addition, Claims 6 and 9 recite that the first and second control terminals are independently controllable. For the reasons stated above, applicant submits that Mizukami does not teach a circuit having first and second control terminals that are independently controllable. In addition, applicant respectfully submits that Mizukami does not suggest first and second control terminals that are independently controllable.

Proebsting fails to overcome the significant shortcomings of Mizukami. As stated above, Proebsting does not disclose or suggest transistors having first and second control terminals that are independently controllable. Additionally, Proebsting offers no suggestion to modify the circuit disclosed therein to arrive at the presently claimed invention and, consequently, the combination proposed by the Examiner does not offer a reasonable chance of success in combining the cited references.

As stated above, Claims 7 and 8 depend from Claim 6, and Claims 10 and 11 depend from Claim 9. Therefore, the comments presented above relating to Claims 6

and 9 apply equally to Claims 7, 8, 10, and 11 which are submitted by applicant to be patentable.

Applicant respectfully contends that the teachings of Mizukami and Proebsting cannot be combined to either teach or suggest each and every feature of the present invention. Therefore, Claims 1, 3, 7, 8, 10, and 11 are believed to be patentably distinguished over the cited references. Applicant respectfully requests that the rejections of Claims 1, 3, 7, 8, 10, and 11 under 35 U.S.C. §103(a) be withdrawn and the claims allowed at this time.

III.B. The Rejection Under 35 U.S.C. §103(a) Over Mizukami In View of Proebsting and Further In View of Taguchi

The Examiner has rejected Claims 4, 5, and 15-17 under 35 U.S.C. §103(a) as being unpatentable over Mizukami in view of Proebsting and further in view of Taguchi. The Examiner contends the cited references teach the recited features of Claims 4, 5, and 15-17 and that it would have been obvious to one of ordinary skill in the art to combine the references to achieve the claimed invention. Official Action, pages 6-8.

Claims 4, 5, and 15 depend from Claim 1. Claim 1 recites (1) an integrated circuit comprising a push-pull driving circuit having a first and second transistor including control terminals being controllably independent by different control pulses between a first and second supply potential; and (2) a single resistor being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type,

wherein the type of the resistor determines, by application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal. Summarily, neither Mizukami, Proebsting, nor Taguchi, alone or in combination, discloses (1) an integrated circuit comprising a push-pull driving circuit having a first and second transistor including control terminals being controllably independent by different control pulses between a first and second supply potential; and (2) a single resistor being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type, wherein the type of the resistor determines, by application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal.

As noted above, Claim 1 recites transistors having first and second control terminals that are independently controllable. In addition, for the reasons provided above, neither Mizukami nor Proebsting disclose or suggest transistors having first and second control terminals that are independently controllable. Further, neither Mizukami nor Proebsting disclose or suggest applying only a single pulse on the output terminal in response to receiving both a positive and negative input pulse, where the single input

pulse is positive or negative depending on whether a single resistor, connected the output terminal, is of a pull-up or pull-down type.

Taguchi fails to overcome the significant shortcomings of Mizukami and Proebsting. Taguchi is directed to a system for transmitting a small-amplitude signal between a microprocessor **5** and a SDRAM **20** via a bus line **15**. Taguchi, column 1, lines 44-48. The system includes a push-pull-type output circuit **12** having a p-channel MOS transistor **13** functioning as a pull-up element and an n-channel MOS transistor **14** functioning as a push-down element. Taguchi, column 1, line 66, to column 2, line 2. As shown in Figure 3, transistors **13** and **14** are coupled in series between a line **26**, which supplies VCC power, and a line **27**, which supplies VSS power. Taguchi, column 2, lines 41-44. Microprocessor **5** includes an output terminal **6** connected to the coupling node of transistors **13** and **14** for connection to bus line **15**. Taguchi, Figure 3. Microprocessor **5** can transmit a low signal to SDRAM **20** by turning transistor **13** off and transistor **14** on. Taguchi, column 2, lines 22-27. Further, microprocessor **5** can transmit a high signal to SDRAM **20** by turning transistor **13** on and transistor **14** off. Taguchi, column 2, lines 27-29. Summarily, the system of Taguchi can transmit either a high or low signal on bus line **15** depending on the signal input into transistors **13** and **14**.

In contrast, the circuit, as claimed in Claim 1, applies only a single pulse on the output terminal in response to receiving both a positive and negative input pulse. The single input pulse is positive or negative depending on whether a single resistor, connected the output terminal, is of a pull-up or pull-down type. Thus, the output and

input signals for the Taguchi system and the circuit of the presently claimed invention differ completely with regard to input and output. Therefore, applicant respectfully submits that Taguchi does not teach or suggest each and every limitation of the presently claimed invention and, thus, cannot anticipate the presently claimed invention. Additionally, Taguchi offers no suggestion to modify the system disclosed therein to arrive at the presently claimed invention and, consequently, the combination proposed by the Examiner does not offer a reasonable chance of success in combining the cited references.

Moreover, the resistors of the presently claimed invention provide an entirely different function than the resistors of the Taguchi system. Regarding Taguchi, the disclosed system includes termination resistors **28**, **29**, **30**, and **31**. Taguchi, column 2, lines 45-50. Taguchi discloses that resistors **28**, **29**, **30**, and **31** are set approximately equal to 50 or 100 ohms. Taguchi, column 2, lines 46, 47, and 51-54. Resistors **28** and **29** and resistors **30** and **31** are connected in series across supply voltages VCC and VSS. Resistors **28**, **29**, **30**, and **31** appear to perform the function of stabilizing the signal differences between lines **15**, **26**, and **27**. In contrast, the single resistor recited in Claim 1 of the present application can be selected to be either a pull-up or pull-down type for determining whether a single positive or a single negative control pulse is applied on the output terminal. The single positive or single negative control pulse is applied on the output terminal in response to the application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the

control terminal of the first transistor. Thus, Taguchi does not teach each and every feature of the presently claimed invention and, thus, cannot anticipate the presently claimed invention. For these additional reasons, it is respectfully submitted that the rejection of amended independent Claim 1 and dependent Claims 4, 5, and 15 should now be withdrawn. Additionally, Taguchi offers no suggestion to modify the system disclosed therein to arrive at the presently claimed invention and, consequently, the combination proposed by the Examiner does not offer a reasonable chance of success in combining the cited references.

As stated above, Claims 4, 5, and 15 depend from Claim 1. Therefore, the comments presented above relating to the patentability of Claim 1 apply equally to Claims 4, 5, and 15.

Claim 16 depends from Claim 6, and Claim 17 depends from Claim 9. Claims 6 and 9 recite a resistor connected between the first supply potential and the output terminal for generating a negative or positive signal pulse at the output terminal in response to the control terminals receiving a sequence of negative and positive control pulses. Applicant respectfully submits that neither Mizukami, Proebsting, nor Taguchi, alone or in combination, disclose a resistor connected between the first supply potential and the output terminal for generating a negative or positive signal pulse at the output terminal in response to the control terminals receiving a sequence of negative and positive control pulses.

As noted above, neither Mizukami nor Proebsting, alone or in combination, disclose or applying only a single pulse on the output terminal in response to receiving both a positive and negative input pulse, where the single input pulse is positive or negative depending on whether a single resistor, connected the output terminal, is of a pull-up or pull-down type. Taguchi fails to overcome the significant shortcomings of Mizukami and Proebsting. As noted above, Taguchi does not disclose or suggest a resistor for generating a negative signal pulse at the output terminal in response to the control terminals receiving a sequence of negative and positive control pulses. Thus, Taguchi does not teach each and every feature of the presently claimed invention and, thus, cannot anticipate the presently claimed invention. For these additional reasons, it is respectfully submitted that the rejection of dependent Claims 16 and 17 should now be withdrawn. Additionally, Taguchi offers no suggestion to modify the system disclosed therein to arrive at the presently claimed invention and, consequently, the combination proposed by the Examiner does not offer a reasonable chance of success in combining the cited references.

As stated above, Claims 16 depends from Claim 6, and Claim 17 depends from Claim 9. Therefore, the comments presented above relating to the patentability of Claims 6 and 9 apply equally to Claims 16 and 17, respectively.

Applicant respectfully submits that the teachings of Mizukami, Proebsting, and Taguchi cannot be combined to either teach or suggest each and every feature of the present invention. Therefore, Claims 4, 5, and 15-17 are believed to be patentably

distinguished over the cited references. Applicant respectfully requests that the rejections of Claims 4, 5, and 15-17 under 35 U.S.C. §103(a) be withdrawn and the claims allowed at this time.

IV. Conclusion

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and such action is earnestly solicited.

If any minor issues should remain outstanding after the Examiner has had an opportunity to study the Amendment and Remarks, it is respectfully requested that the Examiner telephone the undersigned attorney so that all such matters may be resolved and the application placed in condition for allowance without the necessity for another Action and/or Amendment.